

FIG. 1

10

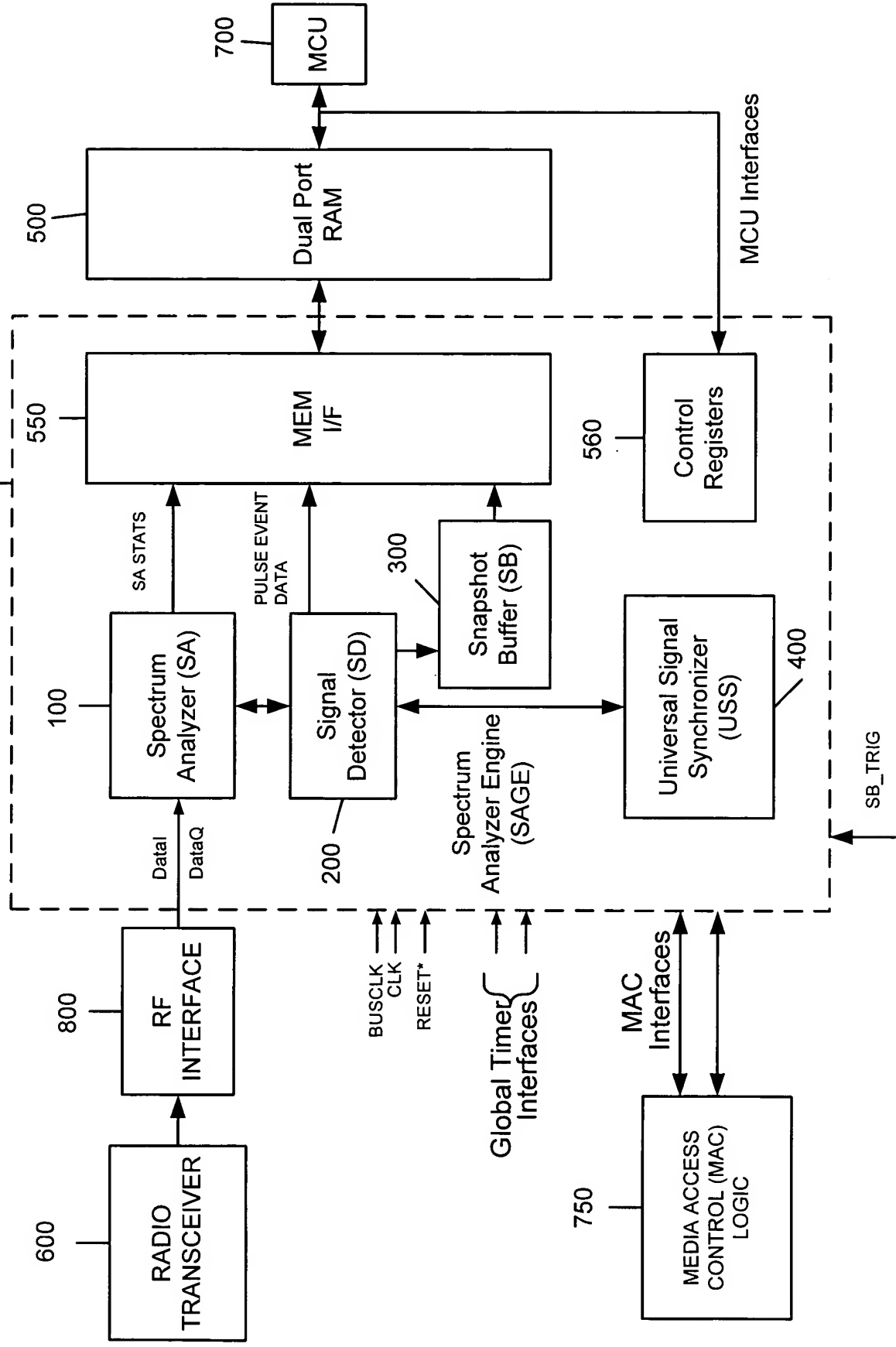


FIG. 2

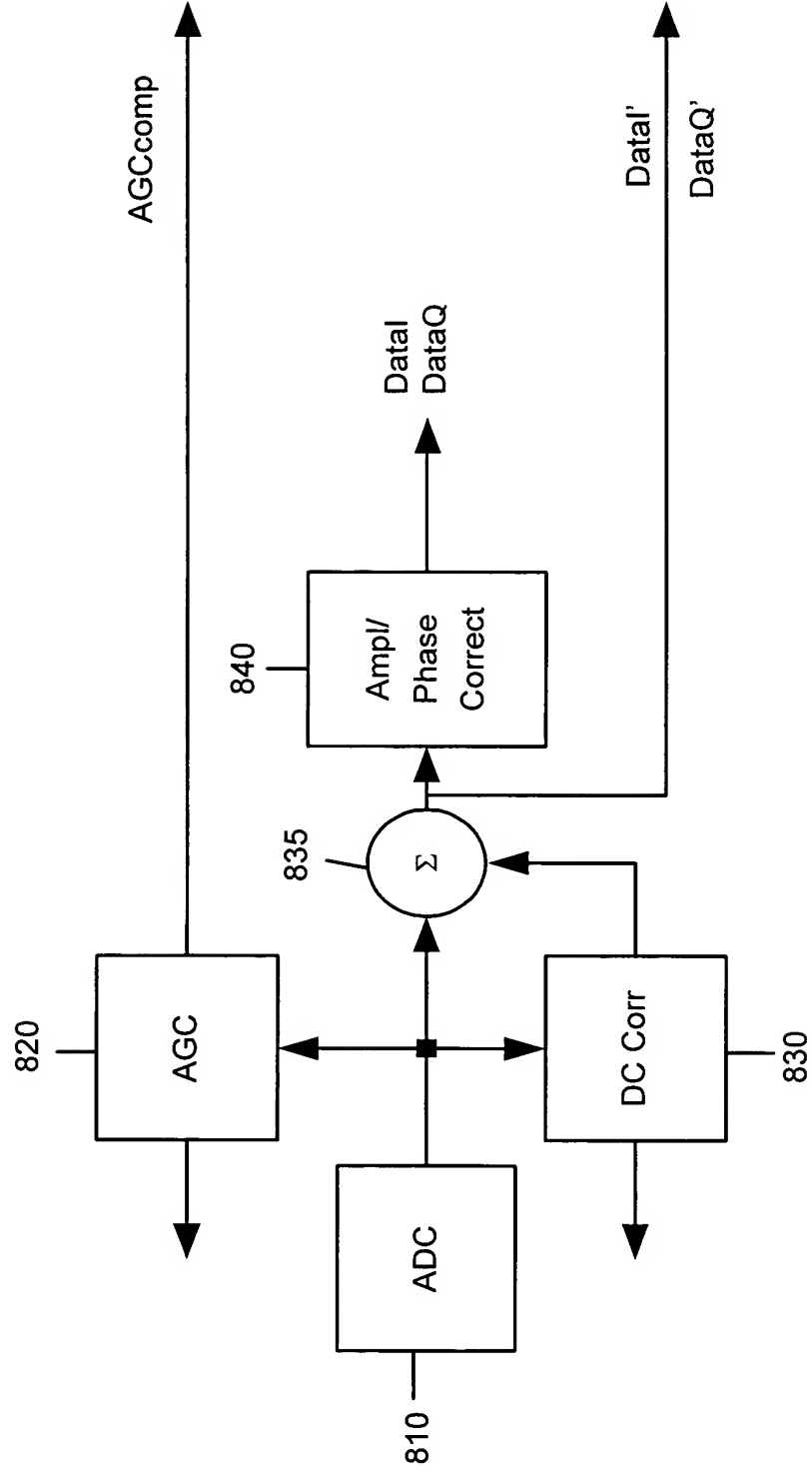


FIG. 3

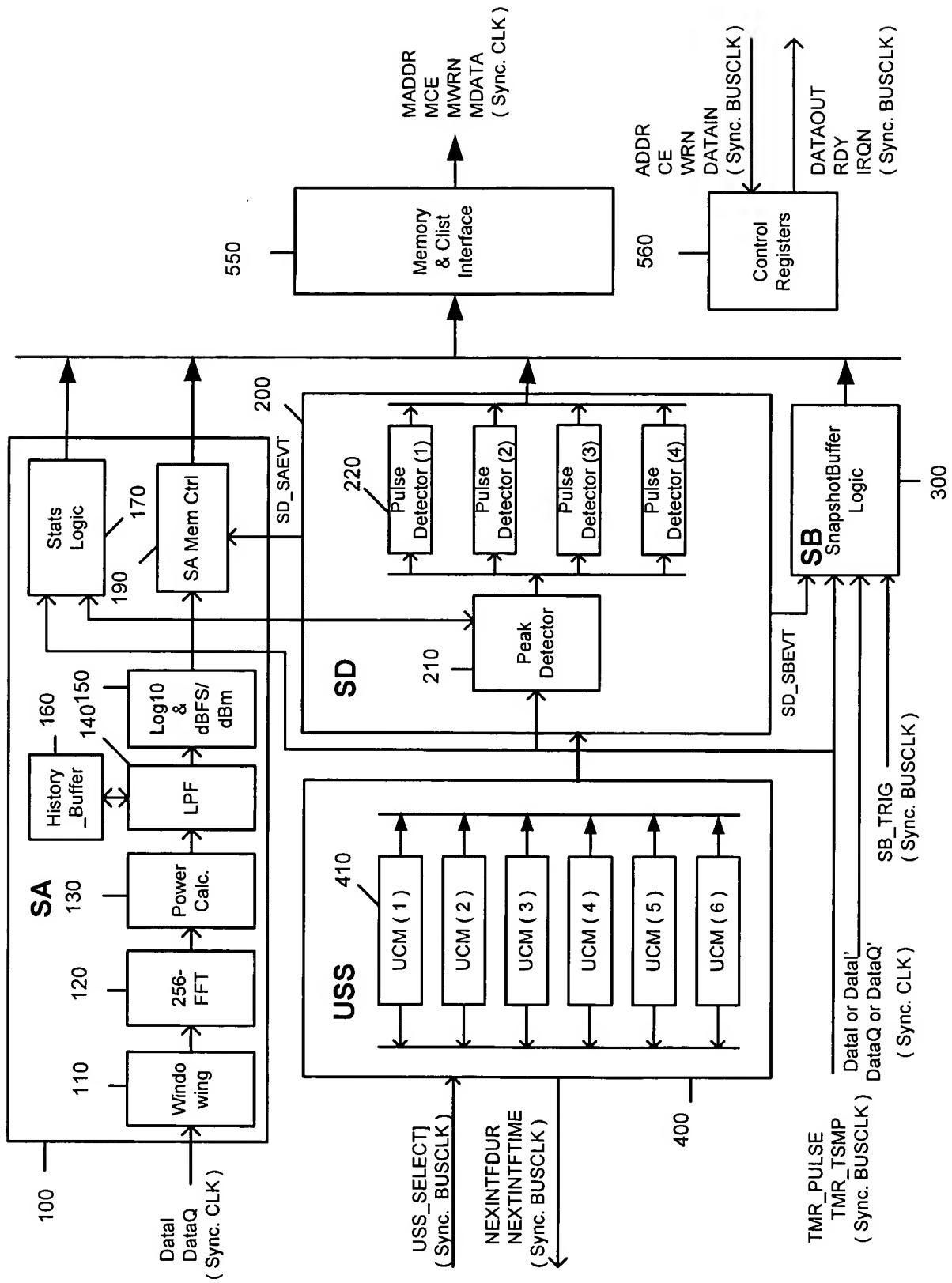


FIG. 4

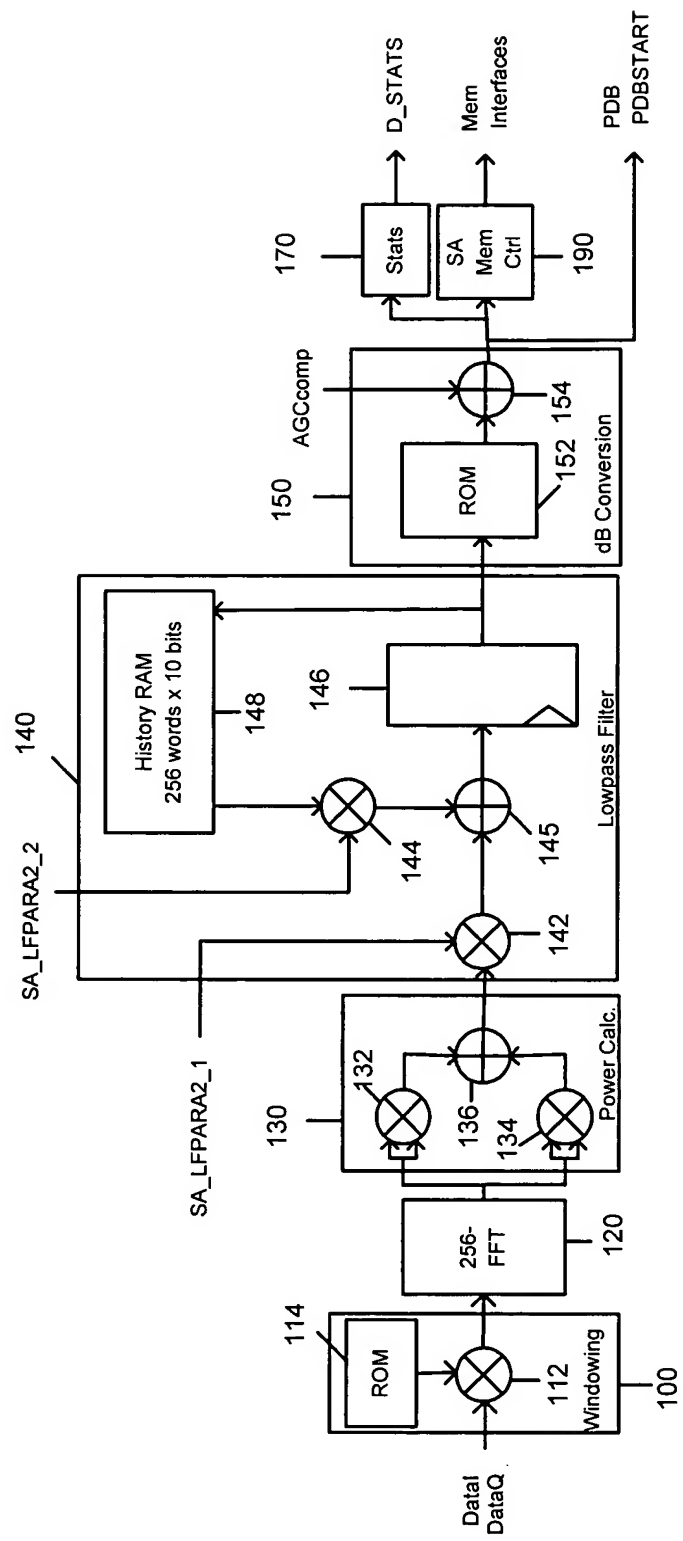




FIG. 6

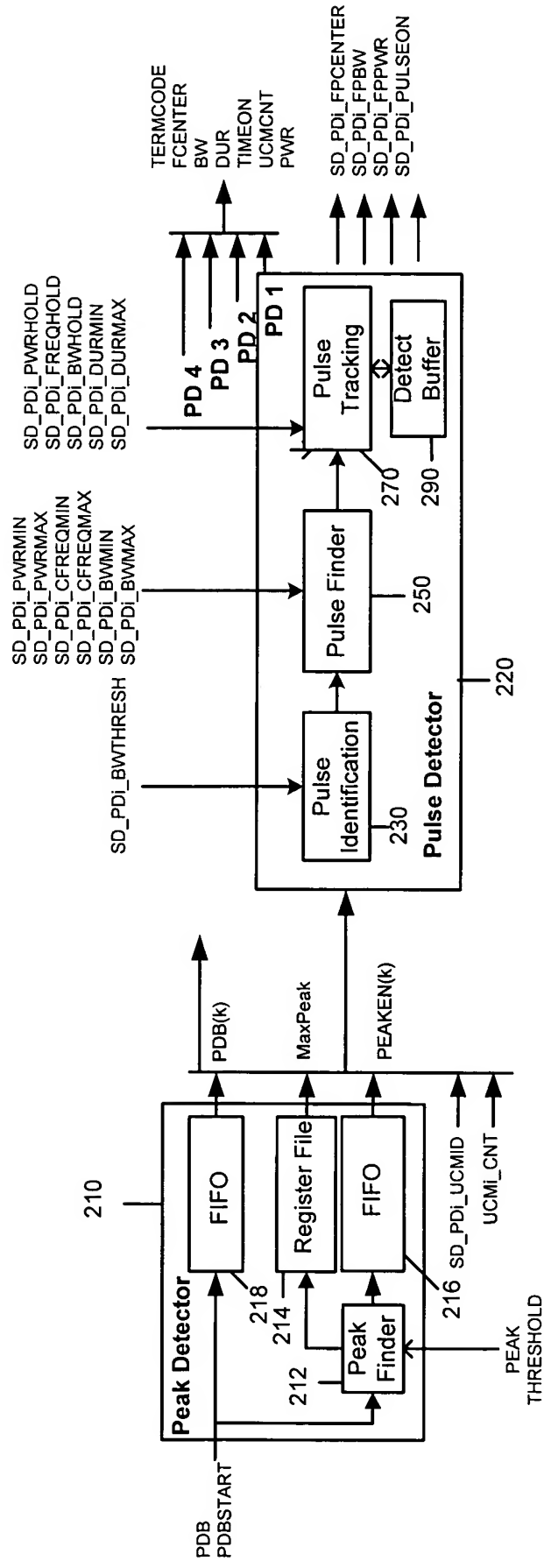


FIG. 7

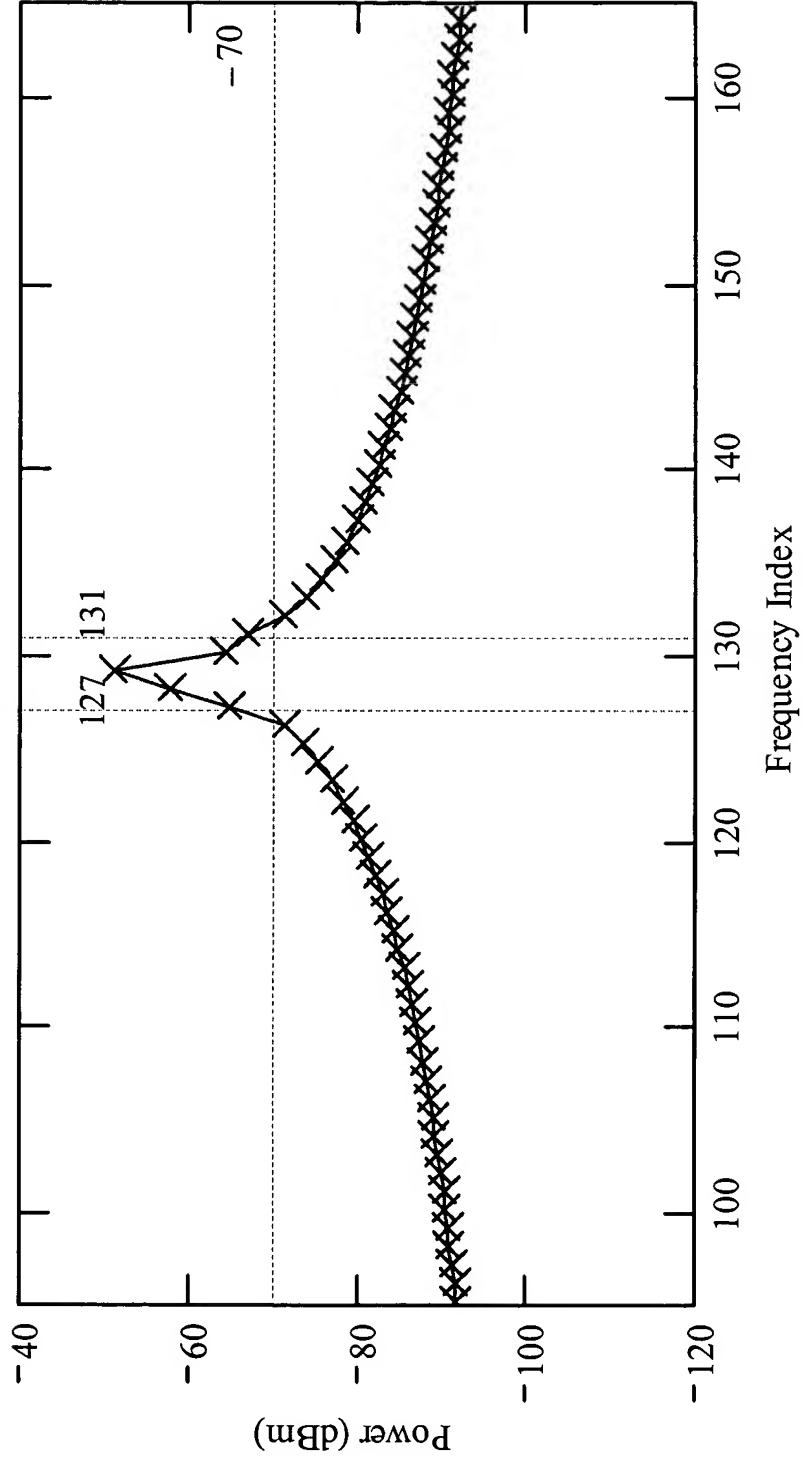


FIG. 8

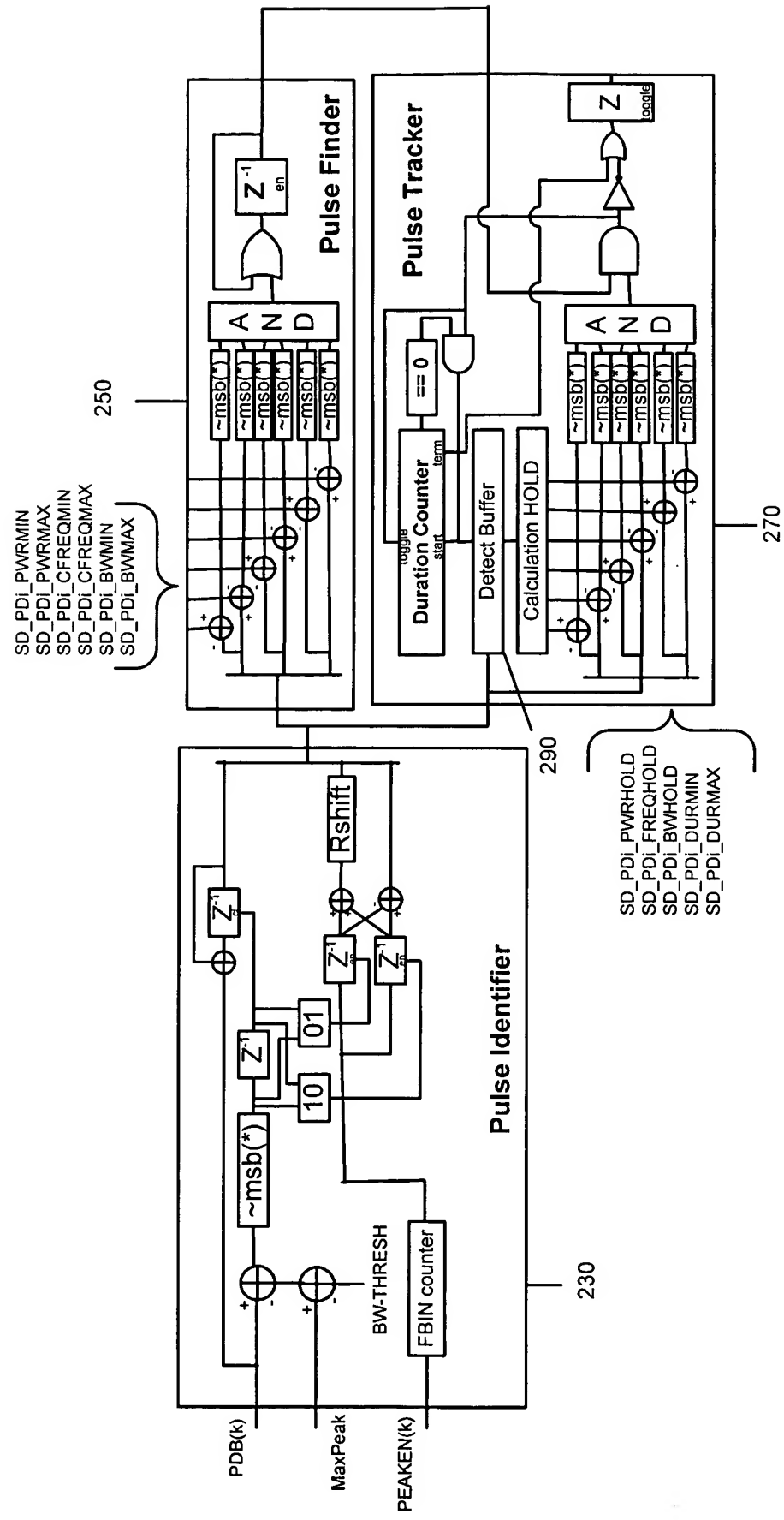




FIG. 9

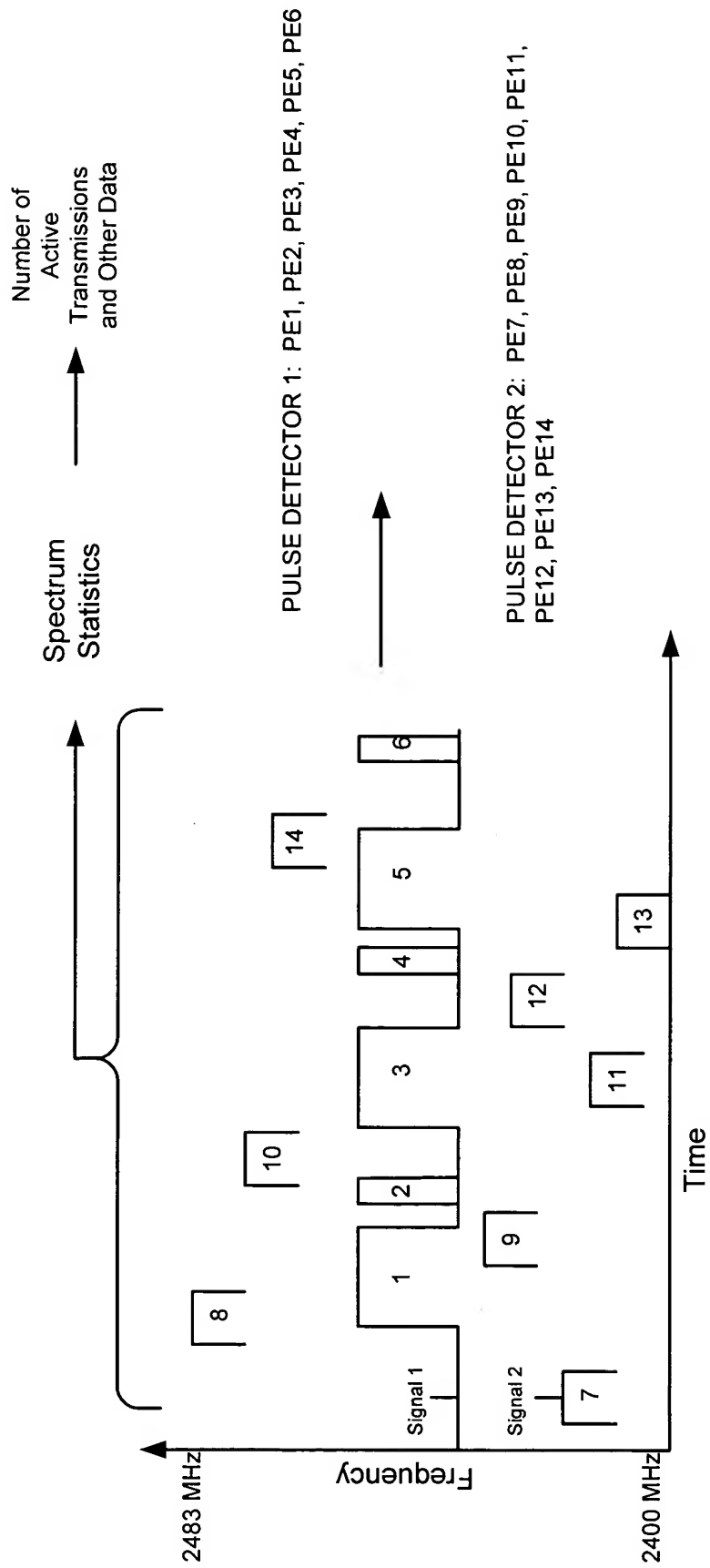


FIG. 10

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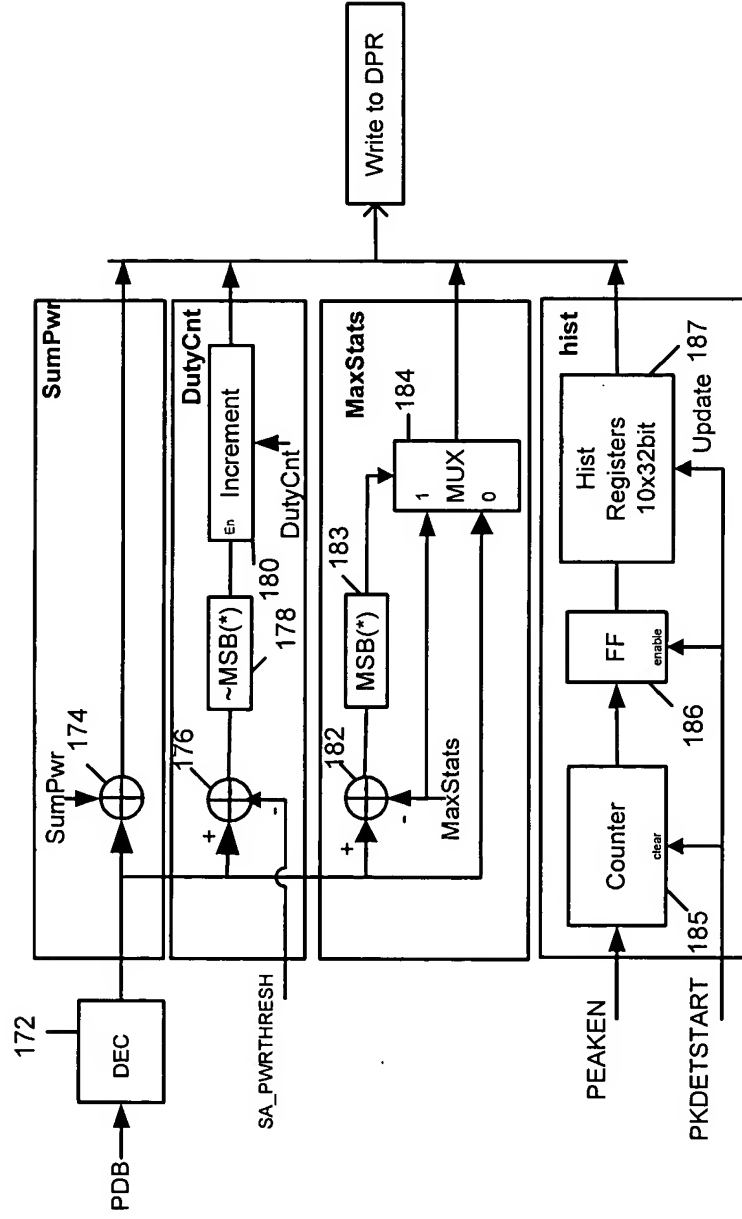


FIG. 11

Time Freq	0	1	2	3	4	5
0	-100	-100	-50	-50	-50	-50
	-100	-100	-50	-50	-50	-50
20	-100	-100	-50	-50	-50	-50
	-100	-100	-100	-100	-100	-100
125	-100	-100	-30	-30	-30	-30
	-100	-100	-30	-30	-30	-30
175	-100	-100	-30	-30	-30	-30
	-100	-100	-100	-100	-100	-100
200	-100	-100	-100	-50	-50	-50
	-100	-100	-100	-50	-50	-50
255	-100	-100	-100	-50	-50	-50



SumPwr	DutyCnt	MaxPwr
-400	4	-50
-400	4	-50
-400	4	-50
-600	0	-100
-320	4	-30
-320	4	-30
-320	4	-30
-600	0	-100
-450	3	-50
-450	3	-50
-450	3	-50

FIG. 12

	Number of Stats Update Cycles With:
No Peaks	2
1 Peak	0
2 Peaks	1
3 Peaks	3
4 Peaks	0
5 Peaks	0
6 Peaks	0
7 Peaks	0
8 Peaks	0
9 Peaks	0

FIG. 13

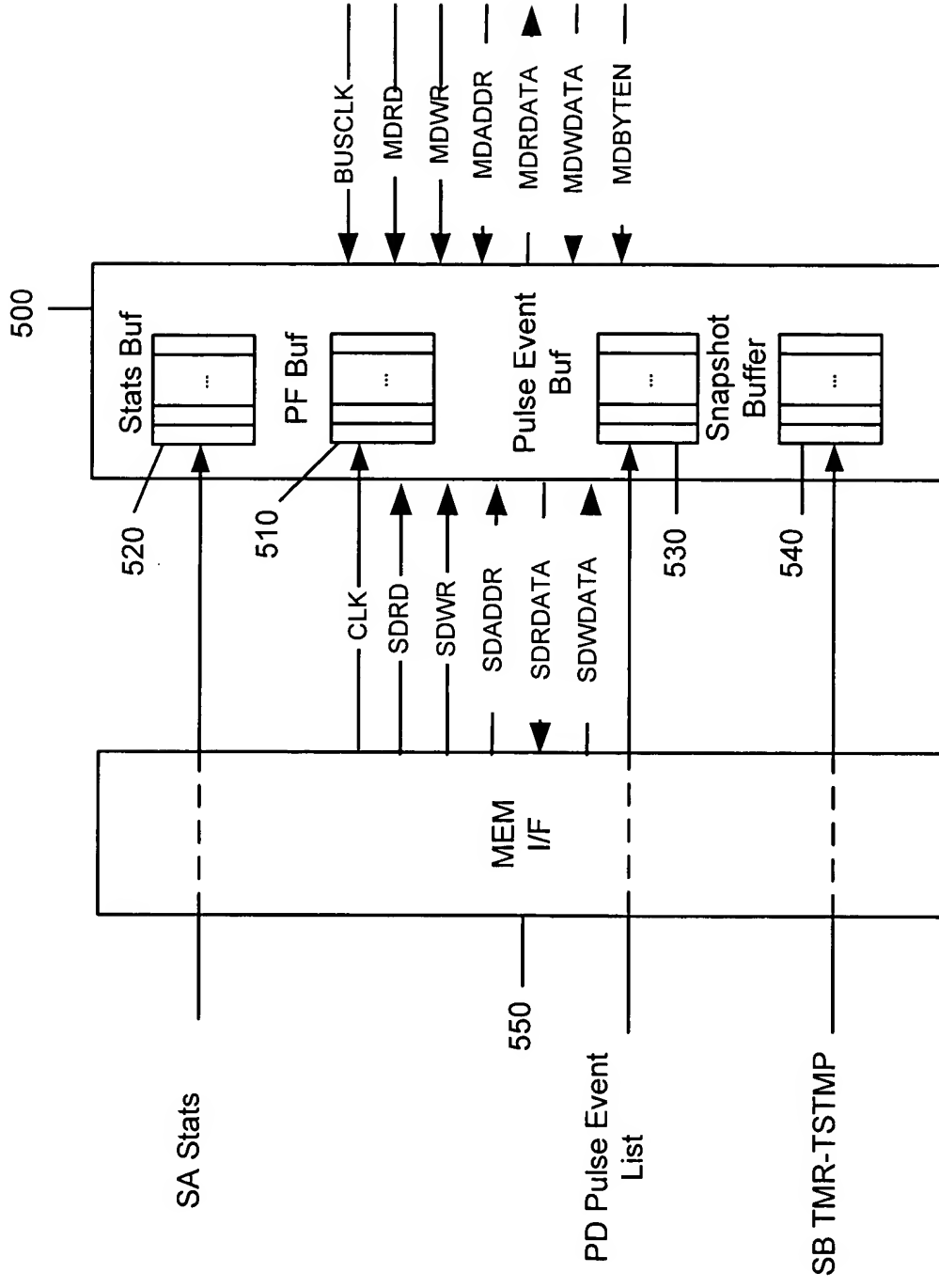


FIG. 14

SAGE Address SDADDR[15:0]	DPR Word (32-bit)	MCU Internal Address	AHB Word Address MDADDR[15:0]	AHB Byte Enable MDBYTEEN[3:0]
0000h	Word 0	XXXX0000h	XXXX0000h	0
0001h	Word 1	XXXX0004h	XXXX0001h	0
0002h	Word 2	XXXX0008h	XXXX0002h	0
FFFFh	Word 65,535	XXX3FFFC h	XXXXFFFFh	0

FIG. 15

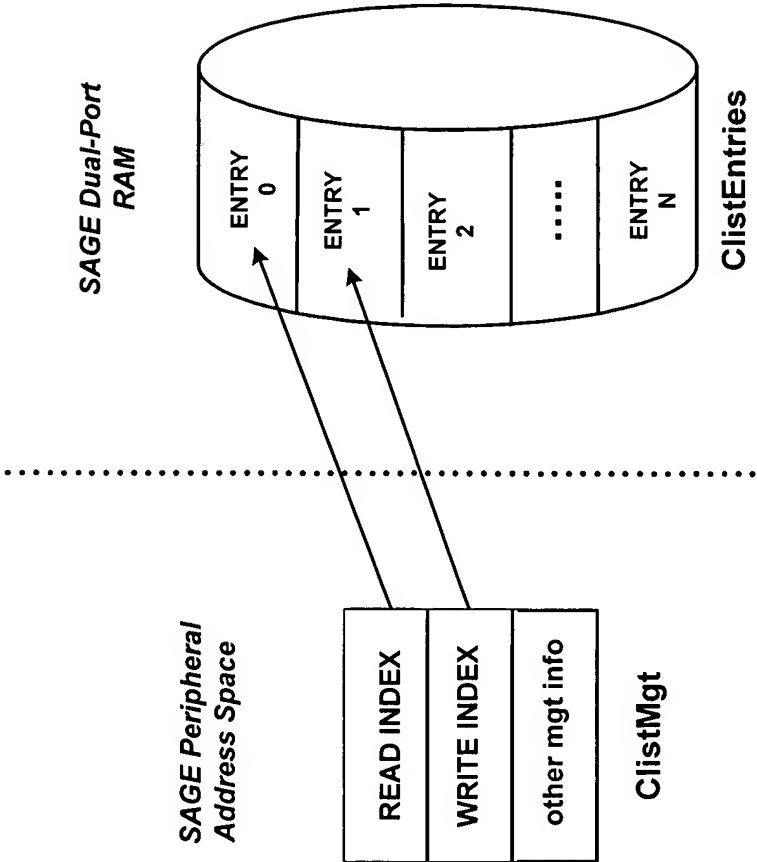


FIG. 16

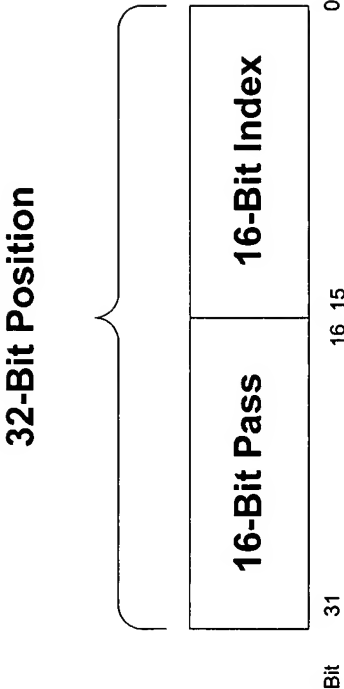


FIG. 17

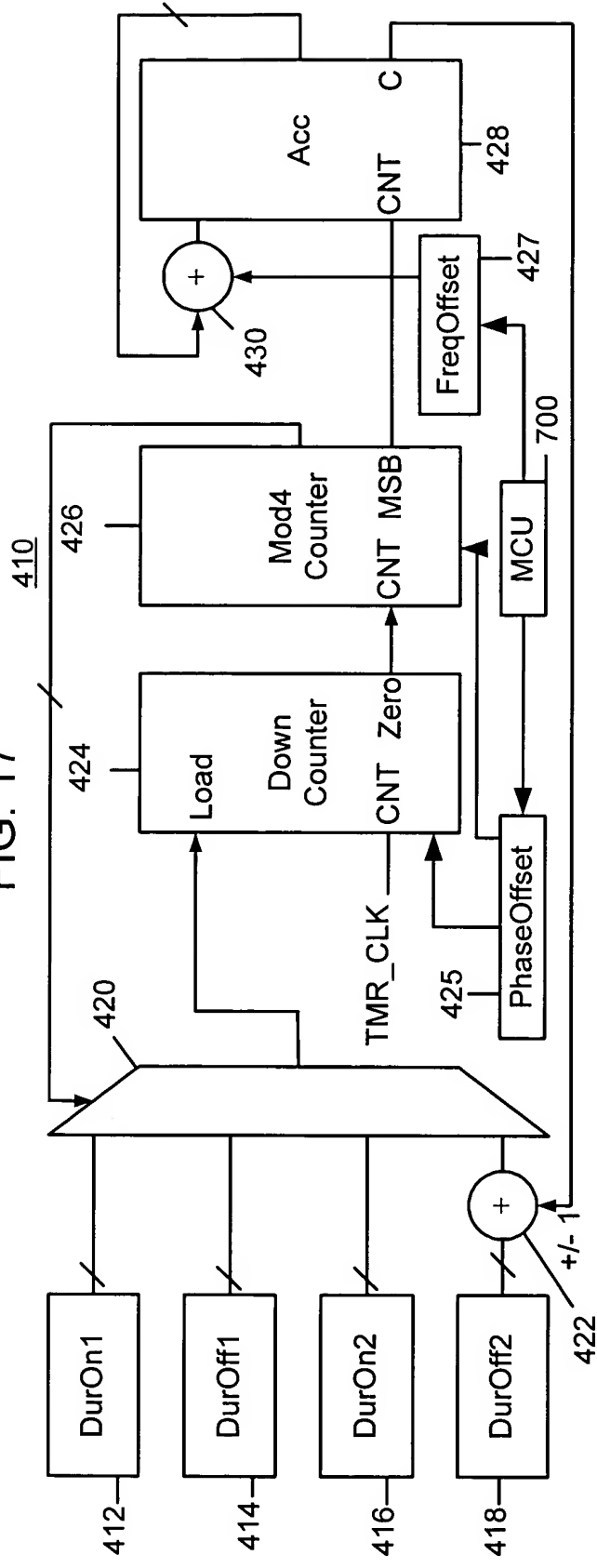


FIG. 18

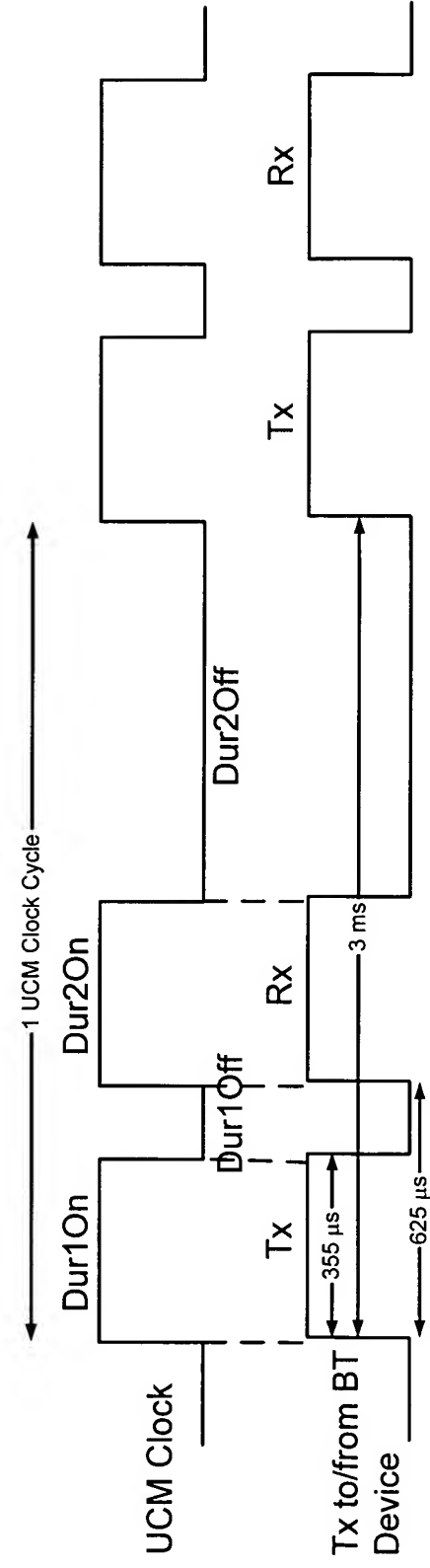




FIG. 19

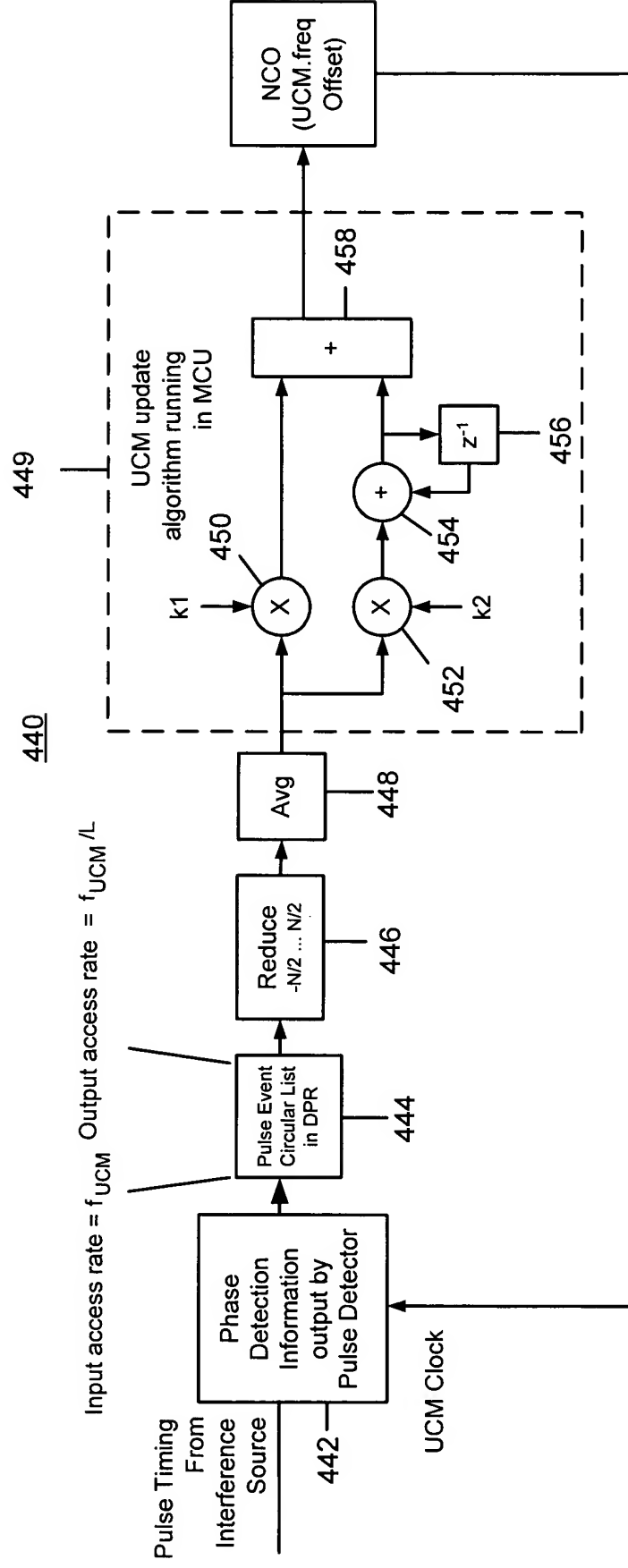


FIG. 20

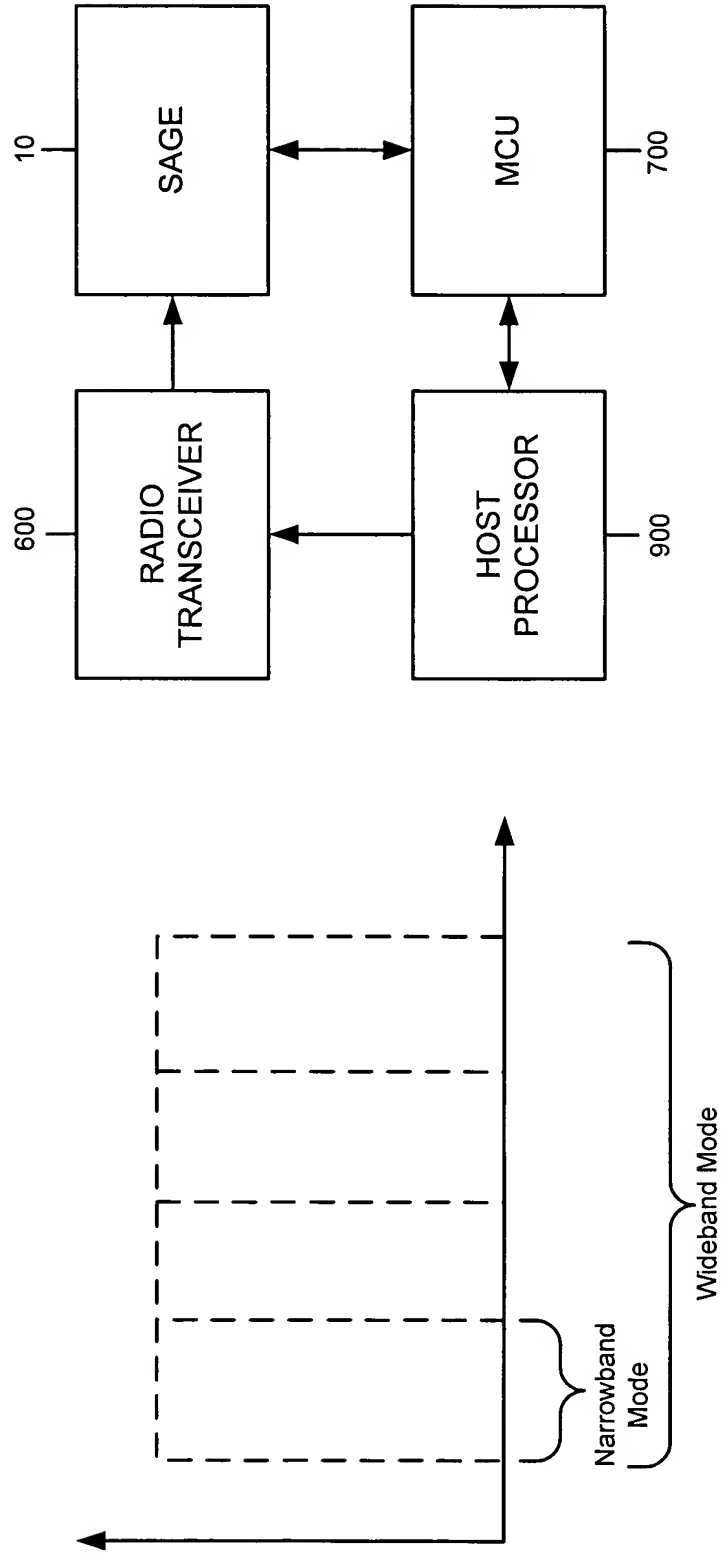


FIG. 21

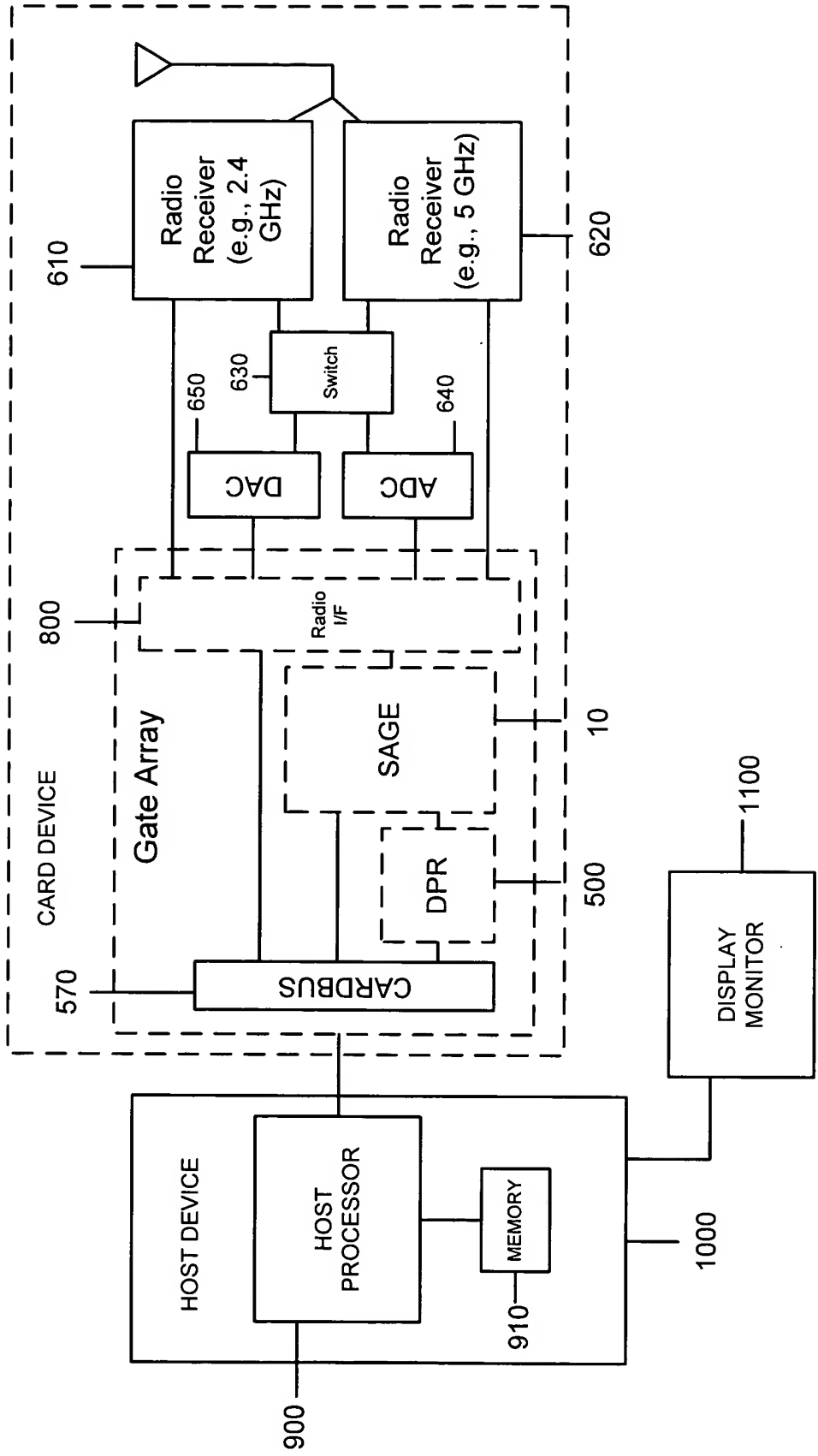


FIG. 22

